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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,273	05/17/2005	Yusuke Otomo	85366	3734

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EXAMINER	
ALMO, KHAREEM E	
ART UNIT	**PAPER NUMBER**
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/535,273	OTOMO ET AL.	
	Examiner	Art Unit	
	Khareem E. Almo	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-12* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The papers filed 10/30/2006 have been received and entered in the case.

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 3-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Holmqvist (US 5220275).

With respect to claim 1, figure 3 of Holmqvist discloses a phase comparator circuit (31, 32, 33, 34, 35 and 36) for operating with a clock signal (reference clock) whose period is 2 times the unit time width of an inputted data signal (input signal), said phase comparator circuit characterized in that; said data signal is inputted to a first latch circuit (31) and a second latch circuit (32), said first latch circuit performs the latching operation thereof with a first clock signal (reference clock), and said second latching circuit performs the latching operation thereof with the second clock signal, as being an inverted clock signal of said first clock signal; the output of said first latching circuit is inputted to a third latch circuit (33), the output of said second latch circuit is inputted to a

fourth latch circuit (34), said third latch circuit performs the latching operation thereof with said second clock signal, and said fourth latch circuit performs the latching operation thereof with said first clock signal; and an exclusive OR (35) of the output from said second latch circuit and the output from said third latch circuit is used as a first phase error signal, and an exclusive OR (36) of the output from said first latch circuit and the output from said fourth latch circuit is used as second phase error signal.

With respect to claim 3, Figure 3 of Holmqvist discloses a phase comparator circuit (31, 32, 33, 34, 35 and 36) for operating with a clock signal whose period is 2 times the unit time width of an inputted data signal (Input signal), said phase comparator circuit characterized in that; a first phase error signal, representing the phase difference between the transition point of said data signal (Input signal), and the rising edge of a first clock signal as the pulse width, is outputted; and a second phase error signal, representing the phase difference between the transition point of said data signal and the rising edge of a second clock signal as being the inverted clock signal of said first clock signal, is outputted.

With respect to claim 4, Figure 3 of Holmqvist discloses the phase comparator circuit (31, 32, 33, 34, 35 and 36) as defined in claim 3, wherein, when the transition has occurred between 2 consecutive data in said data signal (input signal), a first reference signal (clock state), having a time width ranging from the rising edge of said second clock signal to the rising edge of said first clock signal, is outputted in order to determine the increase or the decrease of the pulse width of said first phase error signal; and when the transition has occurred between 2 consecutive data in said data signal, a

second reference signal, having a time width ranging from the rising edge of said first clock signal to the rising edge of said second clock signal (fire signal), is outputted in order to determine the increase or decrease of the pulse width of said second phase error signal.

With respect to claim 5, Figure 3 of Holmqvist discloses a phase comparator circuit (31, 32, 33, 34, 35 and 36) for operating with a clock signal (reference clock) whose period is 2 times the unit time width of an inputted data signal (input signal), said phase comparator circuit characterized in that; the pulse width of the phase error signal representing the phase difference between the transition point of said data signal and the transition point of said clock signal is extended by the time width corresponding to the unit time width of said data signal.

With respect to claim 6, Figure 3 of Holmqvist discloses the phase comparator circuit as defined in claim 5, wherein the first phase error signal, representing the pulse width as being the phase difference between the transition point of the data signal of the even-number sequential order and the rising edge of the said clock signal, is outputted; and the second phase error signal, representing the pulse width as being the phase difference between the transition point of the said data signal of odd-number sequential order and the falling edge of said clock signal, is outputted. (Note the clock signals are complementary and thus give and even and odd sequential order.)

1. Claims 1 and 3-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Summers (GB 2089601).

With respect to claim 1, figure 7 of Summers (GB 2089601) discloses a phase comparator circuit (701-706 and 710) for operating with a clock signal (CK) whose period is 2 times the unit time width of an inputted data signal (DP), said phase comparator circuit characterized in that; said data signal is inputted to a first latch circuit (701) and a second latch circuit (703), said first latch circuit performs the latching operation thereof with a first clock signal (CK), and said second latching circuit performs the latching operation thereof with the second clock signal (CK bar), as being an inverted clock signal of said first clock signal; the output of said first latching circuit is inputted to a third latch circuit (702), the output of said second latch circuit is inputted to a fourth latch circuit (704), said third latch circuit performs the latching operation thereof with said second clock signal, and said fourth latch circuit performs the latching operation thereof with said first clock signal; and an exclusive OR (705) of the output from said second latch circuit and the output from said third latch circuit is used as a first phase error signal, and an exclusive OR (706) of the output from said first latch circuit and the output from said fourth latch circuit is used as second phase error signal.

With respect to claim 3, Figure 7 of Summers discloses a phase comparator circuit (701-706 and 710) for operating with a clock signal whose period is 2 times the unit time width of an inputted data signal (DP), said phase comparator circuit characterized in that; a first phase error signal, representing the phase difference between the transition point of said data signal and the rising edge of a first clock signal as the pulse width, is outputted; and a second phase error signal, representing the phase difference between the transition point of said data signal and the rising edge of a second clock signal as

being the inverted clock signal of said first clock signal, is outputted.

With respect to claim 4, Figures 7 and 9 of Summers discloses a phase comparator circuit as defined in claim 3, wherein, when the transition has occurred between 2 consecutive data in said data signal (DP), a first reference signal (905), having a time width ranging from the rising edge of said second clock signal to the rising edge of said first clock signal (CK), is outputted in order to determine the increase or the decrease of the pulse width of said first phase error signal; and when the transition has occurred between 2 consecutive data in said data signal, a second reference signal (906), having a time width ranging from the rising edge of said first clock signal to the rising edge of said second clock signal, is outputted in order to determine the increase or decrease of the pulse width of said second phase error signal.

With respect to claim 5, Figure 7 of Summers discloses a phase comparator circuit for operating with a clock signal whose period is 2 times the unit time width of an inputted data signal, said phase comparator circuit characterized in that; the pulse width of the phase error signal representing the phase difference between the transition point of said data signal and the transition point of said clock signal is extended by the time width corresponding to the unit time width of said data signal. (Note: the functionality is inherent in the circuit.)

With respect to claim 6, Figure 7 of Summer discloses the phase comparator circuit as defined in claim 5, wherein the first phase error signal (output of 705), representing the pulse width as being the phase difference between the transition point of the data signal (DP) of the even-number sequential (because it is the complement of the odd)

order and the rising edge of the said clock signal (CLK), is outputted; and the second phase error signal (output of 706), representing the pulse width as being the phase difference between the transition point of the said data signal of odd-number sequential (because it is complement of the even) order and the falling edge of said clock signal, is outputted.

With respect to claim 9, Figure 7 of Summers discloses phase comparator circuit (701-706 and 712) for operating with a clock signal whose period is 2 times the unit time width of an inputted data signal, said phase comparator circuit characterized in that; the pulse width of the phase error signal representing the pulse width, as being the phase difference between the transition point of said data signal (DP) and the transition point of said clock signal (CK) , can be extended by any desired time width.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 7-8 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abe (US 5359298) in further view of Summers (GB 2089601 A).

With respect to claim 7, Figure 1 of Abe discloses a CDR circuit including a phase comparator circuit (12 and 22), a charge pump circuit (14 and 24) and a loop filter (16 and 26), operating with a clock signal (CLK) whose period is 2 times the unit time

width of an inputted data signal, and characterized in that; said phase comparator circuit outputs a first phase error signal, representing the pulse width as being the phase difference between the transition point of the said data signal and the rising edge of said clock signal, and a second phase error signal, representing the pulse width as being the phase difference between the transition point of said data signal and the falling edge of said clock signal; when the transition has occurred between two consecutive data in said data signal, said phase comparator circuit outputs a first reference signal, having a time width ranging from the falling edge of said clock signal to the rising edge of said clock signal, and a second reference signal, having a time width ranging from the rising edge of said clock signal to the falling edge of said clock signal; said charge pump circuit comprises a first charge pump (14) circuit for receiving the input of said first phase error signal and the input of said reference signal, and a second charge pump circuit (24) for receiving the input of said second phase error signal and said second reference signal; and the source current to flow into said loop filter according to the said first and second phase error signals and the sink current to flow into said loop filter (16 and 26) according to said first and second reference signals are designed to become equal with each other when the phase of said data signal and the phase of said clock signal coincide with each other but fails to show the details of the phase comparator or the charge pump. Figure 7 of Summers discloses a phase comparator (701-706 and 710) and a charge pump (203 and 707). It would be obvious at the time the invention was made to one of ordinary skill in the art to use the for the purpose of synchronizing the data pulses.

With respect to claim 8 the above combination produces the CDR circuit as defined in claim 7, wherein said charge pump circuit includes a current supply means (708) to be controlled by external voltage ((+) or (-)) so as to adjust the ratio between said source current and said sink current.

With respect to claim 10 the combination above produces a CDR circuit including a phase comparator circuit, a charge pump circuit and a loop filter, operating with a clock signal whose period is 2 times the unit time width of an inputted data signal, and characterized in that; said phase comparator circuit extends the pulse width of the phase error signal, as being the phase difference between the transition point of said data signal ant the transition point of said clock signal, to any desired amount and outputs the phase error signal to said charge pump circuit.

With respect to claim 11, the circuit above produces a phase comparator circuit for operating with a clock signal whose period is equivalent to the unit time width of an inputted data signal multiplied by any natural number, said phase comparator circuit characterized in that; the pulse width of the phase error signal representing the pulse width, as being the phase difference between the transition point of said data signal and the transition point of said clock signal, can be extended by any desired time width.

With respect to claim 12 the combination above produces a CDR circuit including a phase comparator circuit, a charge pump circuit and a loop filter, operating with a clock signal whose period is equivalent to the unit time width of the inputted data signal multiplied by any natural number and characterized in that said phase comparator circuit extends the pulse width of the phase error signal, as being the phase difference

between the transition point of said data signal and the transition point of said clock signal, to any desired amount and outputs the phase error signal to said charge pump circuit.

Allowable Subject Matter

4. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 2, the prior art of record fails to suggest or disclose the phase comparator circuit as defined in claim 1 above wherein the output of the second latch and the output of the first latch are connected to a first and second delay and the exclusive OR output from the 1st delay and the output of the 3rd latch is used as the phase error signal and the exclusive OR output from the 2nd delay and the output of the 4th latch is used as the second phase error signal.

Response to Arguments

5. Applicant's arguments filed 10/30/2006 have been fully considered but they are not persuasive.

In response to applicant's arguments, the recitation "for operating with a clock signal whose period is 2 times the unit time width of an inputted data signal" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

With regard to applicant's arguments Abe neither discloses nor suggest two charge pump circuits wherein the source current flows into a loop filter according to the first and second phase error signals and the sink current flows into the loop filter according to the first and second reference signals and where they are designed to become equal with each other when the phase of the data signal and the phase of the clock signal coincide with each other, the examiner disagrees. The two charge pumps are the charge pumps from Summers. The source current and the sink current are coming from (708 and 709) in Summers and they flow into the loop filter (16 and 26) of Abe. Because the circuit in Abe is a phase lock loop circuit, it is inherently designed such that it reduces phase error signals based off of a reference signal. Because of the updating inherently associated with a phase lock loop, it is further designed such that the input signals gradually become equal with each other. With respect to the mention of the Ck1 and

CK2 clock signals, the Examiner points out that there is solely 1 clock signal mentioned in the claims.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KEA
1/25/2007

Quan Tra
Primary Examiner